ABSTRACT OF THE DISCLOSURE

A system and method are presented for pre-decoding (i.e., determining the address boundaries of) variable-length instructions within an instruction block fetched from memory. The instruction block represents the contents of consecutive addresses in memory, and is fetched in response to a microprocessor request for a specific instruction within the block. After pre-decoding, the instructions present in the block are placed into a cache for execution by the microprocessor. Conventional instruction pre-decoding methods apply only to instructions fetched from addresses at or beyond the address of the requested instruction. The remaining instructions in the block are therefore not utilized. The system and method disclosed herein permit backward pre-decoding of the instruction block, in which the address boundaries of instructions fetched from addresses prior to that of the requested instruction may also be determined. This capability results in more efficient use of the cache.